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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE #5

Applicant : William R. Wheeler et al.
Serial No.: 10/057,193
Filed : January 25, 2002
Assignee : Intel Corporation
Title : GENERATING SIMULATION CODE

Art Unit: 2122
Examiner:

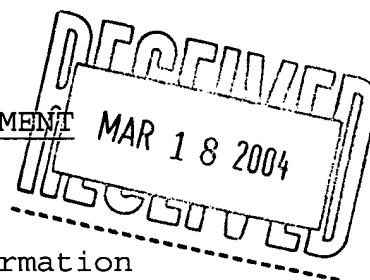
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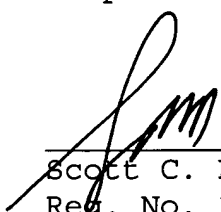
Attorney's Docket No.:10559-604001

Examiner's initials in the left column per MPEP 609 are
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Respectfully submitted,

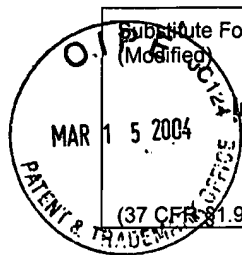
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Substitute Form PTO-1449

U.S. Department of Commerce
Patent and Trademark OfficeAttorney's Docket No.
10559-604001Application No.
10/057,193**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

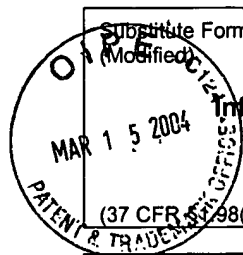
Applicant
William R. Wheeler et al.Filing Date
January 25, 2002Group Art Unit
2122**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
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EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-604001	Application No. 10/057,193
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR 1.98(b))		Applicant William R. Wheeler et al.	
		Filing Date January 25, 2002	Group Art Unit 2122

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Substitute Form PTO-1449 Modified MAR 15 2004 (37 CFR § 1.56(b)) PATENT & TRADEMARK OFFICE	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-604001	Application No. 10/057,193
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	Applicant William R. Wheeler et al.		Filing Date January 25, 2002 Group Art Unit 2122

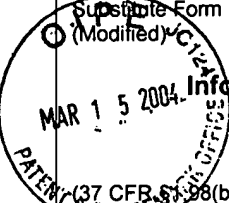
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
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	AQQQ	0 433 066	06/1991	EPO				
	ARRR	0 720 233	07/1996	EPO				
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Foreign Patent Documents or Published Foreign Patent Applications

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							Yes	No
	AAAAA	WO 98/55879	12/1998	WIPO				
	ABBBB	WO 99/39268	08/1999	WIPO				
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	AEEEE	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
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	AOOOO	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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